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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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TESSERA
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EXAMINER	
CAO, PHAT X	
ART UNIT	PAPER NUMBER
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/28/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/786,819	HABA ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-30 and 32-73* is/are pending in the application.

4a) Of the above claim(s) *3,15-19,27,28,30,33 and 44-68* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4-14,20-26,29,32,34-43 and 69-73* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/10/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The cancellation of claims 1 and 31 in Paper filed on 10/10/06 is acknowledged.

Claim Objections

2. Claim 69 is objected to because of the following informalities: in claim 69, last line, "said chip" should be changed to "a chip" because of a first mentioned. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 2, 4-14, 20-21, 29, 32, and 34-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoneda et al (US. 6,376,921).

Regarding claims 2, 4-5, 32, and 34-36, Yoneda (Figs 71 and 81)

discloses a packaged chip comprising: a chip 111 having front and rear surfaces and contacts on the front surface; a coherent, self-supporting chip carrier attached to the chip 111, the chip carrier including a dielectric layer 153 extending across one surface of the chip 111 and having an inner surface facing upwardly and an outer surface facing downwardly, the chip carrier having conductive traces 172 thereon electrically connected to the contacts and conductive bumps 171 formed integrally with the traces 172, the conductive bumps 171 projecting downwardly from the traces, the bumps 171 having bottom ends exposed at the outer surface of the dielectric layer 153 for bonding to contact pads on a circuit panel 250 (not shown in Fig. 71, see Fig. 85 and column 38, lines 58-60), wherein each of the bumps 171 has a first wall portion extending downwardly from one of the traces 172, a bottom wall portion joining the first wall portion adjacent the bottom end of the bump, and a second wall portion extending upwardly from the bottom wall portion to the dielectric layer 153. Yoneda (Fig. 81) further discloses that each of the bumps 171 is generally cup-shaped and formed by filling the metallic film in the through hole (column 26, lines 29-35), with a closed end of the cup shape defining the bottom end of the bump and an open end of the cup shape facing upwardly, the cup-shaped bump 171 further has an imperforate sidewall extending upwardly from the bottom end of the bump 171 to the dielectric layer 153.

Regarding claims 6-8 and 37-39, Yoneda (Fig. 81) also discloses that each bump 171 is substantially solid (i.e., metallic film), has an exterior surface in the form of a surface of revolution about a vertical axis, and has a lead-in surface sloping upwardly

and outwardly around the entire periphery of the bump adjacent the bottom end of the bump.

Regarding claims 9, 11-12, and 40, Yoneda further discloses that all of the bumps 171 are disposed beneath the chip 111 (see Fig. 71) and are disposed in one or more rows (see Fig. 132B) at a pitch of approximately equal to 0.8 mm (column 27, lines 35-36).

Regarding claims 10, 13-14, 29, and 41-43, Yoneda (Fig. 71) further discloses that: the dielectric layer 153 extends beneath the chip 111 and the inner surface of the dielectric layer 153 faces upwardly toward the chip 111; the traces 172 are disposed on the inner side and above the outer side of the dielectric layer 153; and the bumps 171 extend at least partially through the dielectric layer 153 and have bottom ends disposed below the outer surface of the chip carrier.

Regarding claims 20-21, Yoneda (Fig. 71) further discloses that: the upwardly-facing bonding pads 174 on the chip carrier are electrically connected to the traces 172 and bond wires 118 connect the bonding pads 174 to the contact; and a spacer layer 316 of compliant resin (not shown in Fig. 71, see Fig. 132A and column 38, lines 6-10) is disposed between the chip 111 and the dielectric layer 153.

5. Claims 22-26 and 69-73 are rejected under 35 U.S.C. 102(e) as being anticipated by Hashimoto (US. 6,507,095).

Regarding claims 22-24 and 69-71, Hashimoto (Fig. 7 and Fig. 18) discloses a packaged chip comprising: a chip 40 having front and rear surfaces and contacts 44 on the front surface; a coherent, self-supporting chip carrier (10,20) (Fig. 7) or (302,304)

(Fig. 18) attached to the chip, the chip carrier (302,304) including a dielectric layer 302 extending across one surface of the chip 40 and having an inner surface facing upwardly and an outer surface facing downwardly, the chip carrier (302,304) having conductive traces 304 thereon electrically connected to the contacts and conductive bumps 308 formed integrally with the traces 304, the conductive bumps 308 projecting downwardly from the traces 304, the bumps 308 having bottom ends exposed at the outer surface of the dielectric layer 302 for bonding to contact pads on a circuit panel (210,212), wherein the dielectric 302 supports the traces 304 and bumps 308 and wherein the bottom ends of the conductive bumps 308 are movable with respect to the chip (i.e., vertical or horizontal direction) (column 25, lines 6-12).

Regarding claims 25-26 and 72-73, Hashimoto (Fig. 7) further discloses a spacer layer 46 disposed between the chip 40 and the dielectric layer 10, the spacer layer 46 is a compliant insulating resin (column 18, lines 61-64).

Response to Arguments

6. Regarding the rejections of claims 2, 4-14, 20-21, 29, 32, and 34-43, Applicant argues that the conductive bumps of Yoneda are not cup-shaped.

This argument is not persuasive because Fig. 79 clearly teaches the process of forming the cup-shaped conductive bumps 171. Specifically, Yoneda states in column 26, lines 31-35 that:

"the metallic film 160 can be formed by non-electrolytic plating, evaporating or sputtering. During the process of forming the metallic film 160, the metallic film 160 is

filled in the through hole 158, so that the metallic film projection 171 is formed, as shown in Fig. 79."

Therefore, the conductive bumps 171 are cup-shaped because they are formed by filling the metallic film 160 in the through holes 158. The forming of the cup-shaped conductive bumps is also shown in Fig. 84A (top view) and Fig. 85 (cross-sectional view) of an alternative embodiment of Yoneda. Figs. 84A and 85 teach the conductive bumps 213 having a cup-shape, with a closed end of the cup shape defining the bottom end of the bump (Fig. 85) and an open end of the cup shape facing upwardly (Fig. 84A).

Applicant also argues that the chip carrier of Yoneda is not a coherent, self-supporting chip carrier.

This argument is not persuasive because Fig. 81 clearly teaches the forming of the chip carrier itself. Therefore, the chip carrier shown in Fig. 81 is a coherent, self-supporting chip carrier.

Regarding the rejections of claims 22-26 and 69-73, the new reference is applied in the new ground of rejections.

Conclusion

7. This action is made non-final.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PC
December 21, 2006

PHAT X. CAO
PRIMARY EXAMINER